a second diffusion layer of said first transistor coupled to a second contact hole;

a third diffusion layer of said first transistor coupled to a third contact hole;

a main line of a second gate electrode layer of said second transistor extending in said first direction, said second gate electrode layer being electrically separated from said first gate electrode layer;

two branches branching substantially perpendicularly from said main line of said second gate electrode layer, said two branches extending in said second direction;

a fourth diffusion layer of said second transistor coupled to a fourth contact hole, said fourth diffusion layer electrically coupled to said first diffusion layer as said terminal inside of said semiconductor chip;

a fifth diffusion layer of said second transistor coupled to a fifth contact hole; and

a sixth diffusion layer of said second transistor coupled to a sixth contact hole,

wherein said first diffusion layer, one of said branches of said first gate electrode, said second diffusion layer, the other of said branches of said first gate electrode, said third diffusion layer, said fourth diffusion layer, one of said branches of said second gate electrode, said fifth diffusion layer, the other of said branches of said second gate electrode, and said sixth diffusion layer are arranged in this order in a line extending in said first direction.

27. A semiconductor device including first and second transistors formed on a semiconductor chip, each having a terminal commonly connected to a node, said device comprising:

a main line of a first gate electrode layer of said first transistor extending in a first direction;

three branches branching substantially perpendicularly from said main line of said first gate electrode layer, said three branches extending in a second direction;

a first diffusion layer of said first transistor coupled to a first contact hole;

a second diffusion layer of said first transistor coupled to a second contact hole;

a third diffusion layer of said first transistor coupled a third contact hole;

a fourth diffusion layer of said first transistor coupled a fourth contact hole;

a main line of a second gate electrode layer of said second transistor extending in said first direction, said second gate electrode layer being electrically separated from said first gate

electrode layer;

three branches branching substantially perpendicularly from said main line of said second gate electrode layer, said three branches extending in said second direction;

a fifth diffusion layer of said second transistor coupled to a fifth contact hole;

a sixth diffusion layer of said second transistor coupled to a sixth contact hole, said sixth diffusion layer electrically coupled to said second diffusion layer as said terminal inside of said semiconductor chip;

a seventh diffusion layer of said second transistor coupled to a seventh contact hole; and

an eighth diffusion layer of said second transistor coupled to an eighth contact hole,

wherein said first diffusion layer, one of said branches of said first gate electrode, said second diffusion layer, another of said branches of said first gate electrode, said third diffusion layer, the other of said branches of said first gate electrode, said fourth diffusion layer, said fifth diffusion layer, one of said branches of said second gate electrode, said sixth diffusion layer, another of said branches of said second gate electrode, said seventh diffusion layer, the other of said branches of said second gate electrode, and said eighth diffusion layer are arranged in this order in a line extending in said first direction.

28. The device as claimed in claim 26, wherein said first diffusion layer and said third diffusion layer comprise sources of said first transistor,

said second diffusion layer comprises a drain of said first transistor,

said fourth diffusion layer and said sixth diffusion layer comprise sources of said second transistor, and

said fifth diffusion layer comprises a drain of said second transistor.

29. The device as claimed in claim 27, wherein said first diffusion layer and said third diffusion layer comprise sources of said first transistor,

said second diffusion layer and said fourth diffusion layer comprise drains of said first transistor,

said fifth diffusion layer and said seventh diffusion layer comprise sources of said second transistor, and

said sixth diffusion layer and said eighth diffusion layer comprise drains of said

second transistor.

30. The device as claimed in claim 28, further comprising:

a first dummy layer arranged between a third electrode and said fourth diffusion layer;

a second dummy layer arranged so that said first diffusion layer is sandwiched between said second dummy layer and said one of said two branches of said first gate electrode layer; and

a third dummy layer arranged so that said sixth diffusion layer is sandwiched between said third dummy layer and said other of said two branches of said second gate electrode layer.

31. The device as claimed in claim 29, further comprising:

a first dummy layer arranged between said fourth and fifth diffusion layers;

a second dummy layer arranged so that said first diffusion layer is sandwiched between said second dummy layer and said one of said three branches of said first gate electrode layer; and

a third dummy layer arranged so that said eighth diffusion layer is sandwiched between said third dummy layer and said other of said three branches of said second gate electrode layer. --